

Description

BI-DIRECTIONAL MOTOR CONTROL CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a control circuit and, more particularly, to a motor control circuit for controlling an H-bridge drive circuit to operate a bi-directional motor among a forward rotation mode, a brake mode, and a reverse rotation mode.

[0003] 2. Description of the Related Art

[0004] FIG. 1(a) is a detailed circuit diagram showing a conventional motor control circuit 10. FIG. 1(b) is a timing chart showing an operation of the conventional motor control circuit 10. Referring to FIG. 1(a), a bi-directional motor M is connected with an H-bridge drive circuit 1, and the motor control circuit 10 operates the bi-directional motor M among a standby mode, a forward rotation mode, a brake

mode, and a reverse rotation mode through controlling the H-bridge drive circuit 1. More specifically, the H-bridge drive circuit 1 is constructed by six drive transistors Q1 to Q6. A terminal Na of the bi-directional motor M is coupled to a collector electrode of the pnp transistor Q1 and a collector electrode of the npn transistor Q3. A terminal Nb of the bi-directional motor M is coupled to a collector electrode of the pnp transistor Q2 and a collector electrode of the npn transistor Q4. Emitter electrodes of the transistors Q1 and Q2 are connected together to a drive voltage source Vd while emitter electrodes of the transistors Q3 and Q4 are connected together to a ground potential. The transistors Q1 to Q4 are provided with fly-wheel diodes D1 to D4, respectively, for allowing the electromotive force-induced current to flow through when the transistors Q1 to Q4 are turned off. The npn transistor Q5 has a collector electrode coupled to a base electrode of the transistor Q1, and an emitter electrode coupled to a base electrode of the transistor Q4. The npn transistor Q6 has a collector electrode coupled to a base electrode of the transistor Q2 and an emitter electrode coupled to a base electrode of the transistor Q3.

[0005] The motor control circuit 10 has a forward rotation cur-

rent source constructed by a pnp transistor Q7 and a reverse rotation current source constructed by a pnp transistor Q8. The transistor Q7 is biased by a control voltage source Vc1 for providing a control current Ic1. The transistor Q8 is biased by a control voltage source Vc2 for providing a control current Ic2. The control current Ic1 is split at a diverging node N1 into a first partial current If1 and a second partial current If2. The first partial current If1 is supplied to the base electrode of the transistor Q5 while the second partial current If2 is supplied to the base electrode of the transistor Q4. On the other hand, the control current Ic2 is split at a diverging node N2 into a first partial current Ir1 and a second partial current Ir2. The first partial current Ir1 is supplied to the base electrode of the transistor Q6 while the second partial current Ir2 is supplied to the base electrode of the transistor Q3.

[0006] In response to a forward rotation command signal FWD and a reverse rotation command signal REV, the motor control circuit 10 controls the motor drive circuit 1 to operate the motor M among a standby mode, a forward rotation mode, a brake mode, and a reverse rotation mode. Each of the forward and reverse rotation command signals FWD and REV is a logic signal having a HIGH state and a

LOW state. When the forward rotation command signal FWD and the reverse rotation command signal REV are both at the LOW state, npn transistors Q11 and Q12 are turned off. As a result, the control currents I_{c1} and I_{c2} supplied from the control voltage sources V_{c1} and V_{c2} are zero, which may be exemplified by periods T1, T4, and T7 shown in FIG. 1(b). In this case, the motor control circuit 10 is prohibited from supplying the four partial currents I_{f1} , I_{f2} , I_{r1} , and I_{r2} and then makes all of the drive transistors Q1 to Q6 nonconductive, thereby operating the motor M in the standby mode.

[0007] When the forward rotation command signal FWD is at the HIGH state and the reverse rotation command signal REV is at the LOW state, the transistor Q11 is turned on and the transistor Q12 is turned off. The control current I_{c1} supplied from the control voltage source V_{c1} has a maximum I_{c1m} and the control current I_{c2} supplied from the control voltage source V_{c2} is zero, which may be exemplified by period T2 shown in FIG. 1(b). At this time, the first partial current I_{f1} of the control current I_{c1} is allowed to be supplied to the base electrode of the drive transistor Q5 because npn transistor Q9 which is controlled by the reverse rotation command signal REV is turned off. As a

result, the transistors Q1 and Q4 are turned on for allowing a forward current to flow from the terminal Na to the terminal Nb, thereby operating the motor M in the forward rotation mode.

[0008] When the forward rotation command signal FWD and the reverse rotation command signal REV are both at the HIGH state, the transistors Q11 and Q12 are turned on. The control current I_{c1} supplied from the control voltage source V_{c1} has a maximum I_{c1m} and the control current I_{c2} supplied from the control voltage source V_{c2} has a maximum I_{c2m} , which may be exemplified by periods T3 and T6 shown in FIG. 1(b). At this time, the first partial current I_{f1} of the control current I_{c1} is bypassed down to the ground potential through the transistor Q9 which is also turned on by the reverse rotation command signal REV, and therefore prevented from being supplied to the base electrode of the drive transistor Q5. Likely, the first partial current I_{r1} of the control current I_{c2} is bypassed down to the ground potential through the transistor Q10 which is also turned on by the forward rotation command signal FWD, and therefore prevented from being supplied to the base electrode of the drive transistor Q6. However, the second partial current I_{f2} of the control current I_{c1} is

allowed to be supplied to the base electrode of the drive transistor Q4 and the second partial current I_{r2} of the control current I_{c2} is allowed to be supplied to the base electrode of the drive transistor Q3. In this case, the motor current is gradually attenuated to zero when circling in a closed loop composed of the conductive transistors Q3 and Q4 and the motor M, which is referred to as the brake mode.

[0009] When the forward rotation command signal FWD is at the low state and the reverse rotation command signal REV is at the HIGH state, the transistor Q11 is turned off and the transistor Q12 is turned on. As a result, the control current I_{c1} supplied from the control voltage source V_{c1} is zero and the control current I_{c2} supplied from the control voltage source V_{c2} has a maximum I_{c2m} , which may be exemplified by a period T5 shown in FIG. 1(b). At this time, the first partial current I_{r1} of the control current I_{c2} is allowed to be supplied to the base electrode of the drive transistor Q6 because the transistor Q10 which is controlled by the forward rotation command signal FWD is turned off. As a result, the transistors Q2 and Q3 are turned on for allowing a reverse current to flow from the terminal Nb to the terminal Na, thereby operating the mo-

tor M in the reverse rotation mode.

[0010] Although the conventional motor control circuit 10 effectively controls the various operational modes of the motor M, several problems are inevitably caused in its practical applications. Referring to FIG. 1(b), a curve 11 illustrates the control current I_{c1} supplied from the control voltage source V_{c1} of the motor control circuit 10 among the operational modes. As clearly identified in the curve 11, the control voltage source V_{c1} supplies the same control current I_{c1} with the maximum I_{c1m} regardless of the forward rotation mode and the brake mode. However, as described above, the first partial current I_{f1} of the control current I_{c1} in the brake mode is bypassed down to the ground through the conductive transistor Q9 and has nothing to do with controlling the motor drive circuit 1, resulting in a meaningless waste of power. Referring to FIG. 1(b), a curve 12 illustrates the control current I_{c2} supplied from the control voltage source V_{c2} of the motor control circuit 10 among the operational modes. As clearly identified in the curve 12, the control voltage source V_{c2} supplies the same control current I_{c2} with the maximum I_{c2m} regardless of the reverse rotation mode and the brake mode. However, as described above, the first partial current I_{r1}

of the control current I_{c2} in the brake mode is bypassed down to the ground through the conductive transistor Q10 and has nothing to do with controlling the motor drive circuit 1, resulting in a meaningless waste of power.

[0011] Referring to FIG. 1(b), a curve 13 illustrates a total control current consumption of the conventional motor control circuit 10 among the operational modes, i.e. a superposition of the currents I_{c1} and I_{c2} (the curves 11 and 12). As clearly identified in the curve 13, the total control current consumption in the brake mode is twice larger than that in the forward or reverse rotation mode. As described above, the doubling of the total control current consumption is not required by the practical controlling operation and only causes the meaningless waste of power. Therefore, the conventional motor control circuit 10 has a problem with regard to inefficiency and in turn raises operational temperature due to heat generation. A significantly high temperature may cause the circuit malfunction or shut down by thermal protection mechanism.

[0012] Furthermore, the practical magnitude of the control current I_{c1} changes in accordance with the control voltage source V_{c1} since the control current I_{c1} is generated by the control voltage source V_{c1} through the transistor Q7

and the bias resistor. Similarly, the practical magnitude of the control current I_{c2} changes in accordance with the control voltage source V_{c2} since the control current I_{c2} is generated by the control voltage source V_{c2} through the transistor Q8 and the bias resistor. Because the control currents I_{c1} and I_{c2} directly affects the operation points of the drive transistors Q1 to Q6, the fluctuation of the control voltage sources V_{c1} and V_{c2} brings about a problem with regard to operational instability of the motor M.

SUMMARY OF INVENTION

- [0013] In view of the above-mentioned problems, an object of the present invention is to provide a motor control circuit capable of preventing the control currents from being bypassed down to the ground in the brake mode, thereby reducing the power dissipation and suppressing the rise of temperature.
- [0014] Another object of the present invention is to provide a motor control circuit capable of controlling the brake mode by using a relatively low control current, thereby reducing the power dissipation and suppressing the rise of temperature.
- [0015] Still another object of the present invention is to provide a motor control circuit capable of supplying the control cur-

rents by using constant current sources independent of the fluctuation of the control voltage sources, thereby enhancing the operational stability of the motor.

[0016] According to one aspect of the present invention, a motor control circuit is provided for controlling a motor drive circuit to operate a motor among a forward rotation mode, a reverse rotation mode, and a brake mode. The motor control circuit includes a forward rotation control circuit, a reverse rotation control circuit, and a brake control circuit.

[0017] The forward rotation control circuit allows a first current source to supply a first current signal to the motor drive circuit, thereby operating the motor in the forward rotation mode. The reverse rotation control circuit allows a third current source to supply a third current signal to the motor drive circuit, thereby operating the motor in the reverse rotation mode. The brake control circuit allows a second current source and a fourth current source to supply a second current signal and a fourth current signal, respectively, to the motor drive circuit, thereby operating the motor in the brake mode. Since the motor control circuit in the brake mode only allows supplying the second and the fourth current signals, the first and the third cur-

rent signals are prevented from causing undesirable power dissipation.

[0018] Preferably, the second current signal is smaller than the first current signal. The fourth current signal is smaller than the third current signal. The motor control circuit effectively reduces the power dissipation and then suppresses the rise of temperature since the second and the fourth current signals are smaller than the first and the third current signals.

[0019] Preferably, each of the first to fourth current sources is implemented by a constant current source. The operational stability of the motor is enhanced since the first to fourth current signals supplied from the constant current sources are independent of the fluctuation of control voltage sources.

[0020] Preferably, the forward rotation control circuit includes a switch and a logical circuit. The switch is coupled to the first current source. In response to a forward rotation command signal and a reverse rotation command signal, the logical circuit controls the switch for allowing the first current signal to be supplied to the motor drive circuit.

[0021] Preferably, the reverse control circuit includes a switch and a logical circuit. The switch is coupled to the third

current source. In response to a forward rotation command signal and a reverse rotation command signal, the logical circuit controls the switch for allowing the third current signal to be supplied to the motor drive circuit.

[0022] Preferably, the brake control circuit includes a first switch and a second switch. The first switch is coupled to the second current source for allowing the second current signal to be supplied to the motor drive circuit in response to a forward rotation command signal. The second switch is coupled to the fourth current source for allowing the fourth current signal to be supplied to the motor drive circuit in response to a reverse rotation command signal.

BRIEF DESCRIPTION OF DRAWINGS

[0023] The above-mentioned and other objects, features, and advantages of the present invention will become apparent with reference to the following descriptions and accompanying drawings, wherein:

[0024] FIG. 1(a) is a detailed circuit diagram showing a conventional motor control circuit;

[0025] FIG. 1(b) is a timing chart showing an operation of a conventional motor control circuit;

[0026] FIG. 2(a) is a detailed circuit diagram showing a motor control circuit according to a first embodiment of the

present invention;

[0027] FIG. 2(b) is a timing chart showing an operation of a motor control circuit according to a first embodiment of the present invention; and

[0028] FIG. 3 is a detailed circuit diagram showing a motor control circuit according to a second embodiment of the present invention.

DETAILED DESCRIPTION

[0029] The preferred embodiments according to the present invention will be described in detail with reference to the drawings.

[0030] FIG. 2(a) is a detailed circuit diagram showing a motor control circuit 20 according to a first embodiment of the present invention. FIG. 2(b) is a timing chart showing an operation of the motor control circuit 20 according to the first embodiment of the present invention. Referring to FIG. 2(a), a motor M is connected with an H-bridge drive circuit 2, and the motor control circuit 20 operates the motor M among a standby mode, a forward rotation mode, a brake mode, and a reverse rotation mode through controlling the H-bridge drive circuit 2. The H-bridge drive circuit 2 shown in FIG. 2(a) is the same as the H-bridge drive circuit 1 shown in FIG. 1(a) and, for the

sake of simplification, descriptions with regard to the structure and operation of the H-bridge drive circuit 2 will be omitted hereinafter.

[0031] The motor control circuit 20 is provided with four current sources I1 to I4, in which the current sources I1 and I2 are coupled to a control voltage source Vc1 while the current sources I3 and I4 are coupled to a control voltage source Vc2. In one embodiment, the control voltage sources Vc1 and Vc2 are identical with respect to each other. The current source I1 may supply a current twice larger than the current source I2 does while the current source I3 may supply a current twice larger than the current source I4 does. The current from the current source I1 may be set equal in magnitude to that from the current source I3 while the current from the current source I2 may be set equal in magnitude to that from the current source I4. The current source I1 is coupled to the base electrode of the drive transistor Q5 through a switch S1, for supplying a control current signal A. The current source I2 is coupled to the base electrode of the drive transistor Q4 through a switch S2, for supplying a control current signal B. The current source I3 is coupled to the base electrode of the drive transistor Q6 through a switch S3, for supplying a

control current signal C. The current source I4 is coupled to the base electrode of the drive transistor Q3 through a switch S4, for supplying a control current signal D.

[0032] The switch S1 is controlled by an output terminal of a NOR gate NG1. The NOR gate NG1 is employed to perform a NOR logical operation between a forward rotation command signal FWD, after inverted by an inverter INV1, and a reverse rotation command signal REV. The switch S2 is controlled by the forward rotation command signal FWD after inverted by series-connected inverters INV1 and INV2. The switch S3 is controlled by an output terminal of a NOR gate NG2. The NOR gate NG2 is employed to perform a NOR logical operation between a forward rotation command signal FWD and a reverse rotation command signal REV after inverted by an inverter INV3. The switch S4 is controlled by the reverse rotation command signal REV after inverted by series-connected inverters INV3 and INV4.

[0033] Each of the forward and reverse rotation command signals FWD and REV is a logical signal having a HIGH state and a LOW state. When the forward rotation command signal FWD and the reverse rotation command signal REV are both at the LOW state, the NOR gate NG1 outputs LOW for

turning off the switch S1, the inverter INV2 outputs LOW for turning off the switch S2, the NOR gate NG2 outputs LOW for turning off the switch S3, and the inverter INV4 outputs LOW for turning off the switch S4. Since the switches S1 to S4 are all turned off, the current sources I1 to I4 are prevented from supplying any currents, which may be exemplified by periods T1, T4, and T7 shown in FIG. 2(b). In this case, the drive transistors Q1 to Q6 are all turned off, thereby operating the motor M in the standby mode.

[0034] When the forward rotation command signal FWD is at the HIGH state and the reverse rotation command signal REV is at the LOW state, the NOR gate NG1 outputs HIGH for turning on the switch 1, the inverter INV2 outputs HIGH for turning on the switch S2, the NOR gate NG2 outputs LOW for turning off the switch S3, and the inverter INV4 outputs LOW for turning off the switch S4. Since the switches S1 and S2 are both turned on, the current sources I1 and I2 are allowed to supply the control currents to the base electrodes of the transistors Q5 and Q4, respectively, serving as the control current signals A and B. On the other hand, since the switches S3 and S4 are both turned off, the current sources I3 and I4 are pre-

vented from supplying any currents to the base electrodes of the drive transistors Q6 and Q3. As a result, the control current supplied from the control voltage source Vc1 has a magnitude of $I_1 + I_2$ and the control current supplied from the control voltage source Vc2 is zero, which may be exemplified by a period T2 shown in FIG. 2(b). In this case, the drive voltage source Vd supplies a forward current to flow from the terminal Na to the terminal Nb through the conductive transistors Q1 and Q4, thereby operating the motor M in the forward rotation mode.

[0035] When the forward rotation command signal FWD and the reverse rotation command signal REV are both at the HIGH state, the NOR gate NG1 outputs LOW for turning off the switch S1, the inverter INV2 outputs HIGH for turning on the switch S2, the NOR gate NG2 outputs LOW for turning off the switch S3, and the inverter INV4 outputs HIGH for turning on the switch S4. Since the switches S1 and S3 are both turned off, the current sources I1 and I3 are prevented from supplying any currents to the base electrodes of the transistors Q5 and Q6. However, since the switches S2 and S4 are both turned on, the current sources I2 and I4 are allowed to supply the control currents to the base electrodes of the transistors Q4 and Q3, respectively,

serving as the control current signals B and D. As a result, the control current supplied from the control voltage source V_{c1} has a magnitude of I_2 and the control current supplied from the control voltage source V_{c2} has a magnitude of I_4 , which may be exemplified by periods T3 and T6 shown in FIG. 2(b). In this case, the motor current is gradually attenuated to zero when circling in a closed loop consisting of the conductive transistors Q3 and Q4 and the motor M, which is referred to as the brake mode.

[0036] When the forward rotation command signal FWD is at the LOW state and the reverse rotation command signal REV is at the HIGH state, the NOR gate NG1 outputs LOW for turning off the switch S1, the inverter INV2 outputs LOW for turning off the switch S2, the NOR gate NG2 outputs HIGH for turning on the switch S3, and the inverter INV4 outputs HIGH for turning on the switch S4. Since the switches S1 and S2 are both turned off, the current sources I1 and I2 are prevented from supplying currents to the base electrodes of the drive transistors Q5 and Q4. On the other hand, since the switches S3 and S4 are both turned on, the current sources I3 and I4 are allowed to supply the control currents to the base electrodes of the drive transistors Q6 and Q3, respectively, serving as the

control current signals C and D. As a result, the control current supplied from the control voltage source Vc1 is zero and the control current supplied from the control voltage source Vc2 has a magnitude of $I_3 + I_4$, which may be exemplified by a period T5 shown in FIG. 2(b). In this case, the drive voltage Vd supplies a reverse current to flow from the terminal Nb to the terminal Na through the conductive transistors Q2 and Q3, thereby operating the motor M in the reverse rotation mode.

[0037] It should be noted that the motor control circuit 20 according to the first embodiment of the present invention is further provided with resistors Ra and Rb. The resistor Ra is coupled between the base electrode of the drive transistor Q5 and the base electrode of the drive transistor Q4. During a transient period of the switch S1 from conductive to nonconductive, the charge accumulated between the base and emitter electrodes of the drive transistor Q5 may be removed through the resistor Ra and therefore the drive transistor Q5 is turned off more rapidly. Similarly, the resistor Rb is coupled between the base electrode of the drive transistor Q6 and the base electrode of the drive transistor Q3. During a transient period of the switch S3 from conductive to nonconductive,

the charge accumulated between the base and emitter electrodes of the drive transistor Q6 may be removed through the resistor Rb and therefore the drive transistor Q5 is turned off more rapidly.

[0038] As described above, the motor control circuit 20 according to the first embodiment of the present invention effectively controls the motor M among the forward rotation mode, the brake mode, and the reverse rotation mode. In addition, the motor control circuit 20 provides the following advantages. Firstly, in one embodiment, each of the current sources I1 to I4 may be implemented by a constant current source which supplies the corresponding one of the control current signals A to D independent of the fluctuation of the control voltage sources Vc1 and Vc2. Therefore, the motor control circuit 20 enhances the operational stability of the motor M.

[0039] Referring to FIG. 2(b), a curve 21 illustrates the control current supplied from the control voltage source Vc1 of the motor control circuit 20 among the operational modes. As clearly identified in the curve 21, the control voltage source Vc1 in the brake mode is required to supply a single current I2 only, in contrast with two currents I1 and I2 required in the forward rotation mode. More—

over, the single control current I_2 from the control voltage source V_{c1} in the brake mode is completely applied to drive the transistor Q4 without being bypassed down to the ground. Therefore, the motor control circuit 20 according to the present invention eliminates the meaningless waste of power and effectively suppresses the rise of temperature. Referring to FIG. 2(b), a curve 22 illustrates the control current supplied from the control voltage source V_{c2} of the motor control circuit 20 among the operational modes. As clearly identified in the curve 22, the control voltage source V_{c2} in the brake mode is required to supply a single current I_4 only, in contrast with two currents I_3 and I_4 required in the reverse rotation mode. Moreover, the single control current I_4 from the control voltage source V_{c2} in the brake mode is completely applied to drive the transistor Q3 without being bypassed down to the ground. Therefore, the motor control circuit 20 according to the present invention eliminates the meaningless waste of power and effectively suppresses the rise of temperature. Referring to FIG. 2(b), a curve 23 illustrates a total control current consumption of the motor control circuit 20 among the operational modes, i.e. a superposition of the control currents from the control

voltage sources V_{c1} and V_{c2} (the curves 21 and 22). As clearly identified in the curve 23, the total control current consumption in the brake mode is two third smaller than that in the forward or reverse rotation mode. Therefore, the motor control circuit 20 achieves a highly efficient operation.

[0040] FIG. 3 is a detailed circuit diagram showing a motor control circuit 30 according to a second embodiment of the present invention. Referring to FIG. 3, the motor control circuit 30 generates four control current signals A to D from four current sources, respectively, in response to a forward rotation command signal FWD and a reverse rotation command signal REV. Pnp transistors P1 to P8 form a current source having multiple parallel output stages, coupled to a control voltage source V_c , for providing a reference current I_{ref} to other components in the circuit. The transistors P1 and P2 form a Darlington pair. The transistors P3 and P8, serving as the multiple current output stages, have base electrodes all connected to a base electrode of the transistor P1.

[0041] First is described in detail how the motor control circuit 30 generates the control current signal A. A collector electrode of the transistor P6 supplies the reference cur-

rent I_{ref} to a collector electrode of npn transistor W1. Npn transistors W1 and W2 form a current mirror, in which the transistor W1 has its base electrode coupled to its collector electrode. In one embodiment, the transistor W2 may be designed to have an emitter size twice larger than that of the transistor W1, for supplying a twice-larger reference current. Npn transistors Aa to Ae form a current source, functioning as the current source I1 shown in FIG. 2(a). More specifically, the transistors Aa and Ab form a current mirror, in which the transistor Aa has its base electrode coupled to its collector electrode. The transistors Ac to Ae form a current output stage for amplifying the current from a collector electrode of the transistor Ab as the control current signal A. The current mirror formed by the transistors W1 and W2, functioning as the switch S1 shown in FIG. 2(a), is controlled in accordance with the forward and reverse rotation command signals FWD and REV through npn transistors V1, G1, and G2. More specifically, the transistor V1 functions as the inverter INV1 shown in FIG. 2(a) and the transistors G1 and G2 together function as the NOR gate NG1 shown in FIG. 2(a). A base electrode of the transistor V1 is coupled to receive the forward rotation command signal FWD, a base electrode

of the transistor G1 is coupled to a collector electrode of the transistor V1, and a base electrode of the transistor G2 is coupled to receive the reverse rotation command signal REV. Collector electrodes of the transistors G1 and G2 are together coupled to the base electrodes of the transistors W1 and W2. When the forward rotation command signal FWD is at the HIGH state and the reverse rotation command signal REV is at the LOW state, the transistors G1 and G2 are both turned off. The reference current I_{ref} is allowed to pass the current mirror formed by the transistors W1 and W2 and then be supplied to the current source formed by the transistors Aa to Ae. In this case, the current source formed by the transistors Aa to Ae is allowed to output a predetermined current, serving as the control current signal A. When the forward rotation command signal FWD is at the LOW state, the transistor G1 is turned on to make the transistors W1 and W2 non-conductive. As a result, the reference current I_{ref} is prevented from being supplied to the current source formed by the transistors Aa to Ae. In this case, the current source formed by the transistors Aa to Ae is prohibited from supplying any currents.

[0042] Subsequently is described in detail how the motor control

circuit 30 generates the control current signal B. A collector electrode of the transistor P7 supplies the reference current I_{ref} to a collector electrode of npn transistor W3. Npn transistors W3 and W4 form a current mirror, in which the transistor W3 has its base electrode coupled to its collector electrode. In one embodiment, the transistor W4 may be designed to have an emitter size equal to that of the transistor W3, for supplying the same reference current. Npn transistors Ba to Bc form a current source, functioning as the current source I2 shown in FIG. 2(a). More specifically, the transistors Ba and Bb form a current mirror, in which the transistor Ba has its base electrode coupled to its collector electrode. The transistor Bc forms a current output stage for amplifying the current from a collector electrode of the transistor Bb as the control current signal B. The current mirror formed by the transistors W3 and W4, functioning as the switch S2 shown in FIG. 2(a), is controlled in accordance with the forward rotation command signal FWD through npn transistors V1 and V2. More specifically, the transistor V1 functions as the inverter INV1 shown in FIG. 2(a) and the transistor V2 functions as the inverter INV2 shown in FIG. 2(a). A base electrode of the transistor V1 is coupled to receive the for-

ward rotation command signal FWD and a base electrode of the transistor V2 is coupled to a collector electrode of the transistor V1. A collector electrode of the transistor V2 is coupled to the base electrodes of the transistors W3 and W4. When the forward rotation command signal FWD is at the HIGH state, the transistor V2 is turned off. The reference current I_{ref} is allowed to pass the current mirror formed by the transistors W3 and W4 and then be supplied to the current source formed by the transistors Ba to Bc. In this case, the current source formed by the transistors Ba to Bc is allowed to output a predetermined current, serving as the control current signal B. When the forward rotation command signal FWD is at the LOW state, the transistor V2 is turned on to make the transistors W3 and W4 nonconductive. As a result, the reference current I_{ref} is prevented from being supplied to the current source formed by the transistors Ba to Bc. In this case, the current source formed by the transistors Ba to Bc is prohibited from supplying any currents.

[0043] Subsequently is described in detail how the motor control circuit 30 generates the control current signal C. A collector electrode of the transistor P5 supplies the reference current I_{ref} to a collector electrode of npn transistor W5.

Npn transistors W5 and W6 form a current mirror, in which the transistor W5 has its base electrode coupled to its collector electrode. In one embodiment, the transistor W6 may be designed to have an emitter size twice larger than that of the transistor W5, for supplying a twice-larger reference current. Npn transistors Ca to Ce form a current source, functioning as the current source I3 shown in FIG. 2(a). More specifically, the transistors Ca and Cb form a current mirror, in which the transistor Ca has its base electrode coupled to its collector electrode. The transistors Cc to Ce form a current output stage for amplifying the current from a collector electrode of the transistor Cb as the control current signal C. The current mirror formed by the transistors W5 and W6, functioning as the switch S3 shown in FIG. 2(a), is controlled in accordance with the forward and reverse rotation command signals FWD and REV through npn transistors V3, G3, and G4. More specifically, the transistor V3 functions as the inverter INV3 shown in FIG. 2(a) and the transistors G3 and G4 together function as the NOR gate NG2 shown in FIG. 2(a). A base electrode of the transistor V3 is coupled to receive the reverse rotation command signal REV, a base electrode of the transistor G3 is coupled to a collector electrode of the

transistor V3, and a base electrode of the transistor G4 is coupled to receive the forward rotation command signal FWD. Collector electrodes of the transistors G3 and G4 are together coupled to the base electrodes of the transistors W5 and W6. When the reverse rotation command signal REV is at the HIGH state and the forward rotation command signal FWD is at the LOW state, the transistors G3 and G4 are both turned off. The reference current I_{ref} is allowed to pass the current mirror formed by the transistors W5 and W6 and then be supplied to the current source formed by the transistors Ca to Ce. In this case, the current source formed by the transistors Ca to Ce is allowed to output a predetermined current, serving as the control current signal C. When the reverse rotation command signal REV is at the LOW state, the transistor G3 is turned on to make the transistors W5 and W6 nonconductive. As a result, the reference current I_{ref} is prevented from being supplied to the current source formed by the transistors Ca to Ce. In this case, the current source formed by the transistors Ca to Ce is prohibited from supplying any currents.

[0044] Subsequently is described in detail how the motor control circuit 30 generates the control current signal D. A collec-

tor electrode of the transistor P4 supplies the reference current I_{ref} to a collector electrode of npn transistor W7. Npn transistors W7 and W8 form a current mirror, in which the transistor W7 has its base electrode coupled to its collector electrode. In one embodiment, the transistor W8 may be designed to have an emitter size equal to that of the transistor W7, for supplying the same reference current. Npn transistors Da to Dc form a current source, functioning as the current source I4 shown in FIG. 2(a). More specifically, the transistors Da and Db form a current mirror, in which the transistor Da has its base electrode coupled to its collector electrode. The transistor Dc forms a current output stage for amplifying the current from a collector electrode of the transistor Db as the control current signal D. The current mirror formed by the transistors W7 and W8, functioning as the switch S4 shown in FIG. 2(a), is controlled in accordance with the reverse rotation command signal REV through npn transistors V3 and V4. More specifically, the transistor V3 functions as the inverter INV3 shown in FIG. 2(a) and the transistor V4 functions as the inverter INV4 shown in FIG. 2(a). A base electrode of the transistor V3 is coupled to receive the reverse rotation command signal REV and a base electrode of the

transistor V4 is coupled to a collector electrode of the transistor V3. A collector electrode of the transistor V4 is coupled to the base electrodes of the transistors W7 and W8. When the reverse rotation command signal REV is at the HIGH state, the transistor V4 is turned off. The reference current I_{ref} is allowed to pass the current mirror formed by the transistors W7 and W8 and then be supplied to the current source formed by the transistors Da to Dc. In this case, the current source formed by the transistors Da to Dc is allowed to output a predetermined current, serving as the control current signal D. When the reverse rotation command signal REV is at the LOW state, the transistor V4 is turned on to make the transistors W7 and W8 nonconductive. As a result, the reference current I_{ref} is prevented from being supplied to the current source formed by the transistors Da to Dc. In this case, the current source formed by the transistors Da to Dc is prohibited from supplying any currents.

[0045] While the invention has been described by way of examples and in terms of preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications. Therefore, the scope of the

appended claims should be accorded the broadest interpretation so as to encompass all such modifications.